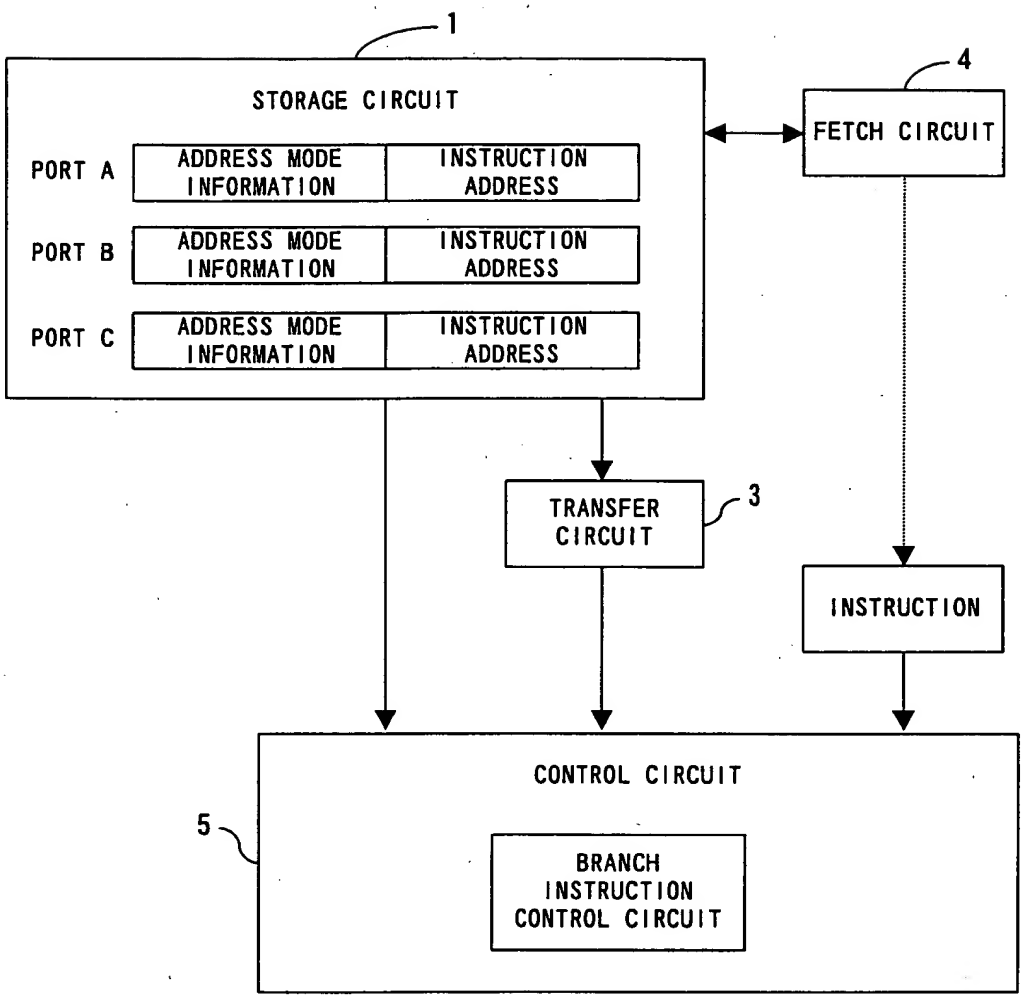

1
STORAGE CIRCUIT
PORT A
ADDRESS MODE INFORMATION
INSTRUCTION ADDRESS
PORT B
ADDRESS MODE INFORMATION
INSTRUCTION ADDRESS
PORT C
ADDRESS MODE INFORMATION
INSTRUCTION ADDRESS
4
FETCH CIRCUIT
TRANSFER CIRCUIT
3
INSTRUCTION
CONTROL CIRCUIT
5
BRANCH INSTRUCTION CONTROL CIRCUIT

FIG. 1

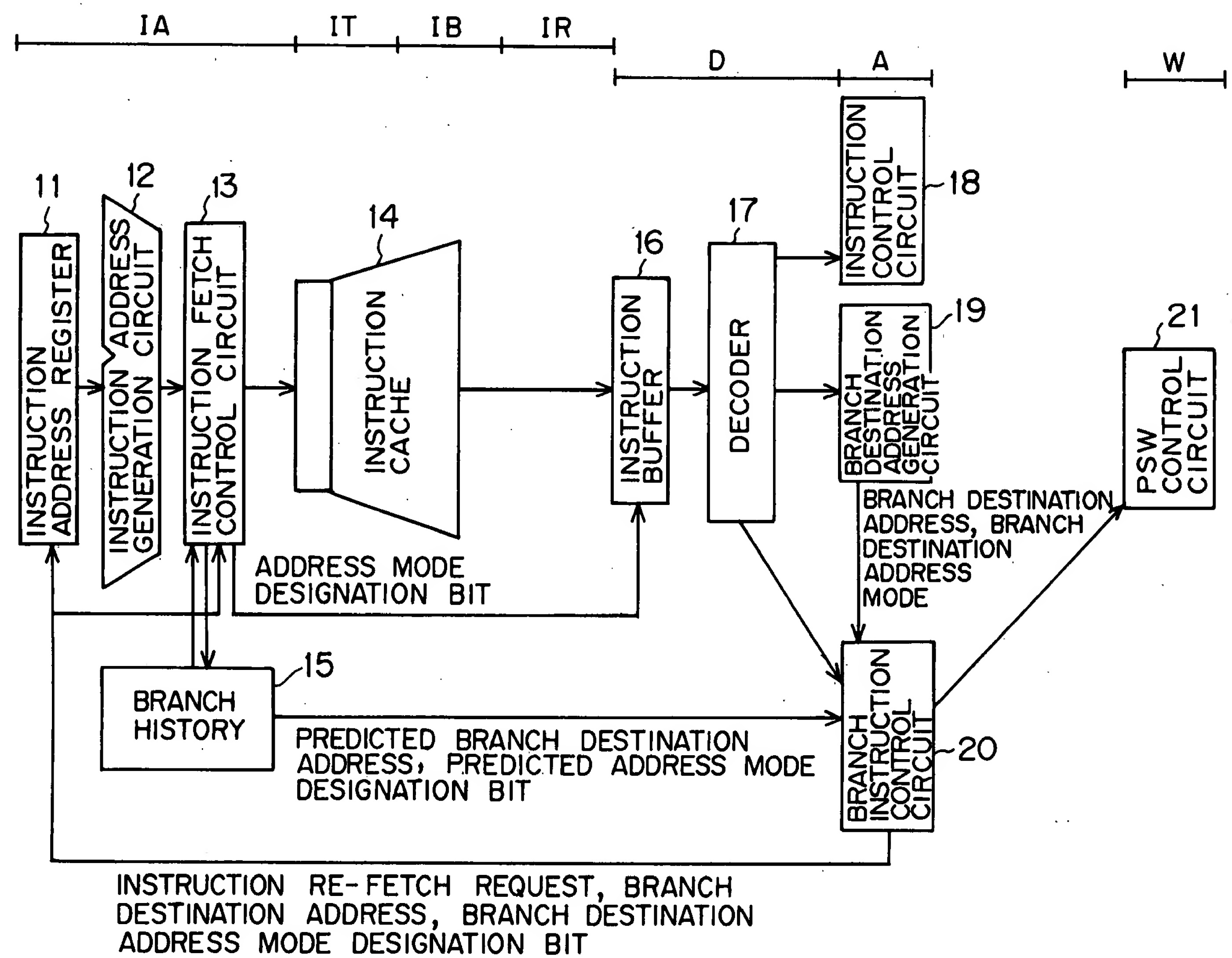

IA
IT
IB
IR
D
A
W
11
INSTRUCTION ADDRESS REGISTER
12
INSTRUCTION ADDRESS GENERATION CIRCUIT
13
INSTRUCTION FETCH CONTROL CIRCUIT
14
INSTRUCTION CACHE
16
INSTRUCTION BUFFER
17
DECODER
18
INSTRUCTION CONTROL CIRCUIT
19
BRANCH DESTINATION ADDRESS GENERATION CIRCUIT
21
PSW CONTROL CIRCUIT
ADDRESS MODE DESIGNATION BIT
15
BRANCH HISTORY
BRANCH DESTINATION ADDRESS, BRANCH DESTINATION ADDRESS MODE
PREDICTED BRANCH DESTINATION ADDRESS, PREDICTED ADDRESS MODE DESIGNATION BIT
20
BRANCH INSTRUCTION CONTROL CIRCUIT
INSTRUCTION RE-FETCH REQUEST, BRANCH DESTINATION ADDRESS, BRANCH DESTINATION ADDRESS MODE DESIGNATION BIT

FIG. 2

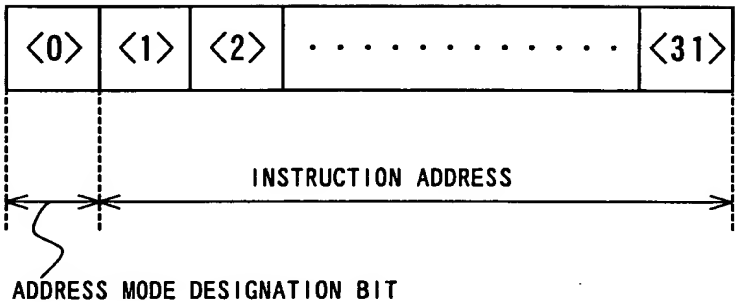


FIG. 3

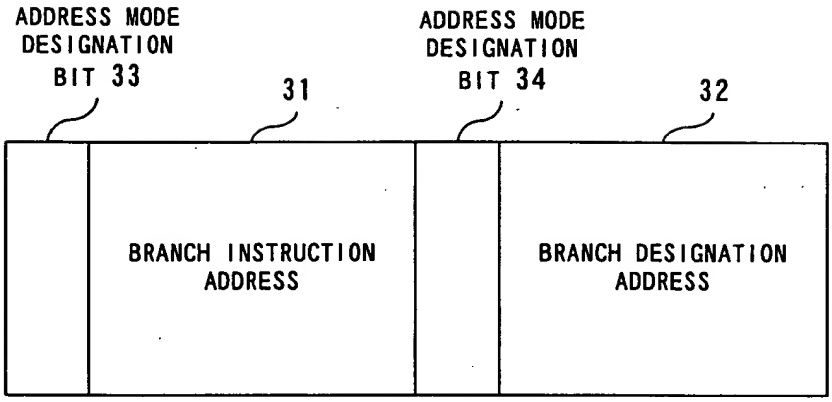

ADDRESS MODE
DESIGNATION
BIT 33
31
ADDRESS MODE
DESIGNATION
BIT 34
32
BRANCH INSTRUCTION
ADDRESS
BRANCH DESIGNATION
ADDRESS

FIG. 4

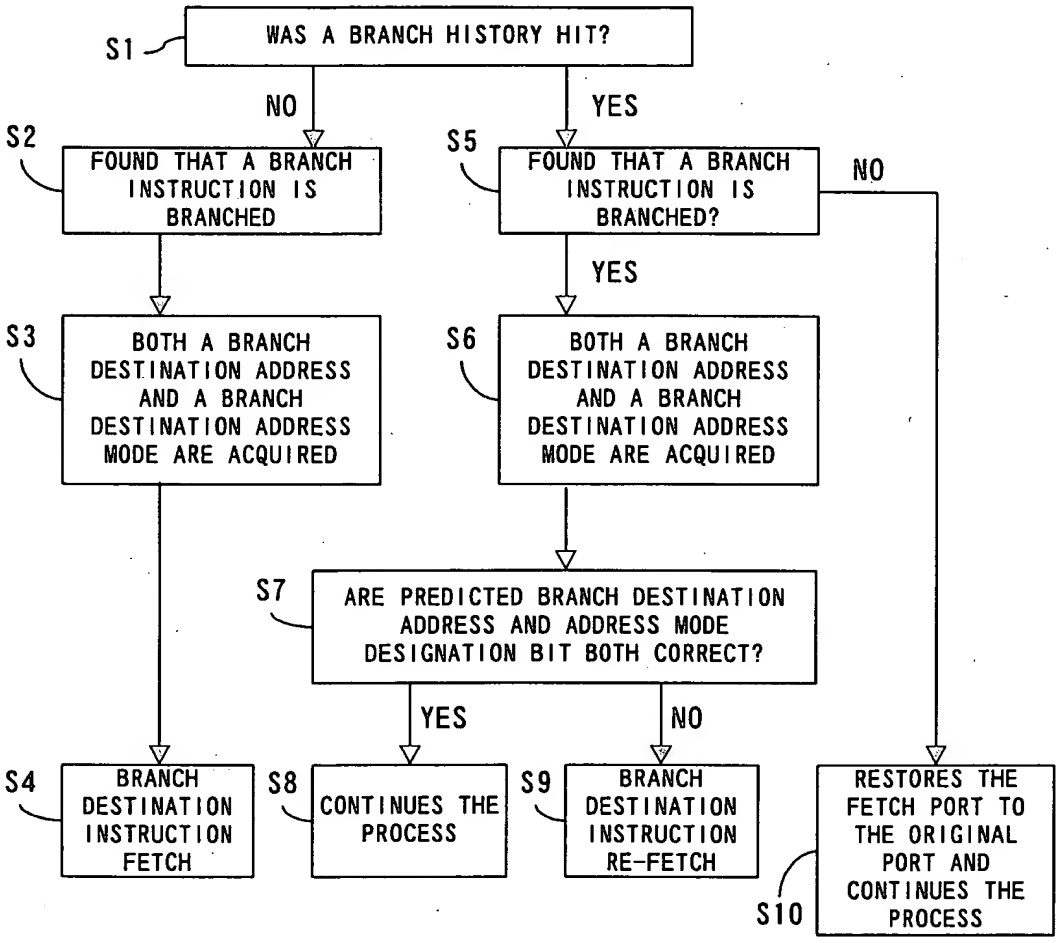

S1
WAS A BRANCH HISTORY HIT?
NO
YES
S2
FOUND THAT A BRANCH INSTRUCTION IS BRANCHED
S5
FOUND THAT A BRANCH INSTRUCTION IS BRANCHED?
NO
YES
S3
BOTH A BRANCH DESTINATION ADDRESS AND A BRANCH DESTINATION ADDRESS MODE ARE ACQUIRED
S6
BOTH A BRANCH DESTINATION ADDRESS AND A BRANCH DESTINATION ADDRESS MODE ARE ACQUIRED
S7
ARE PREDICTED BRANCH DESTINATION ADDRESS AND ADDRESS MODE DESIGNATION BIT BOTH CORRECT?
YES
NO
S4
BRANCH DESTINATION INSTRUCTION FETCH
S8
CONTINUES THE PROCESS
S9
BRANCH DESTINATION INSTRUCTION RE-FETCH
S10
RESTORES THE FETCH PORT TO THE ORIGINAL PORT AND CONTINUES THE PROCESS

FIG. 5

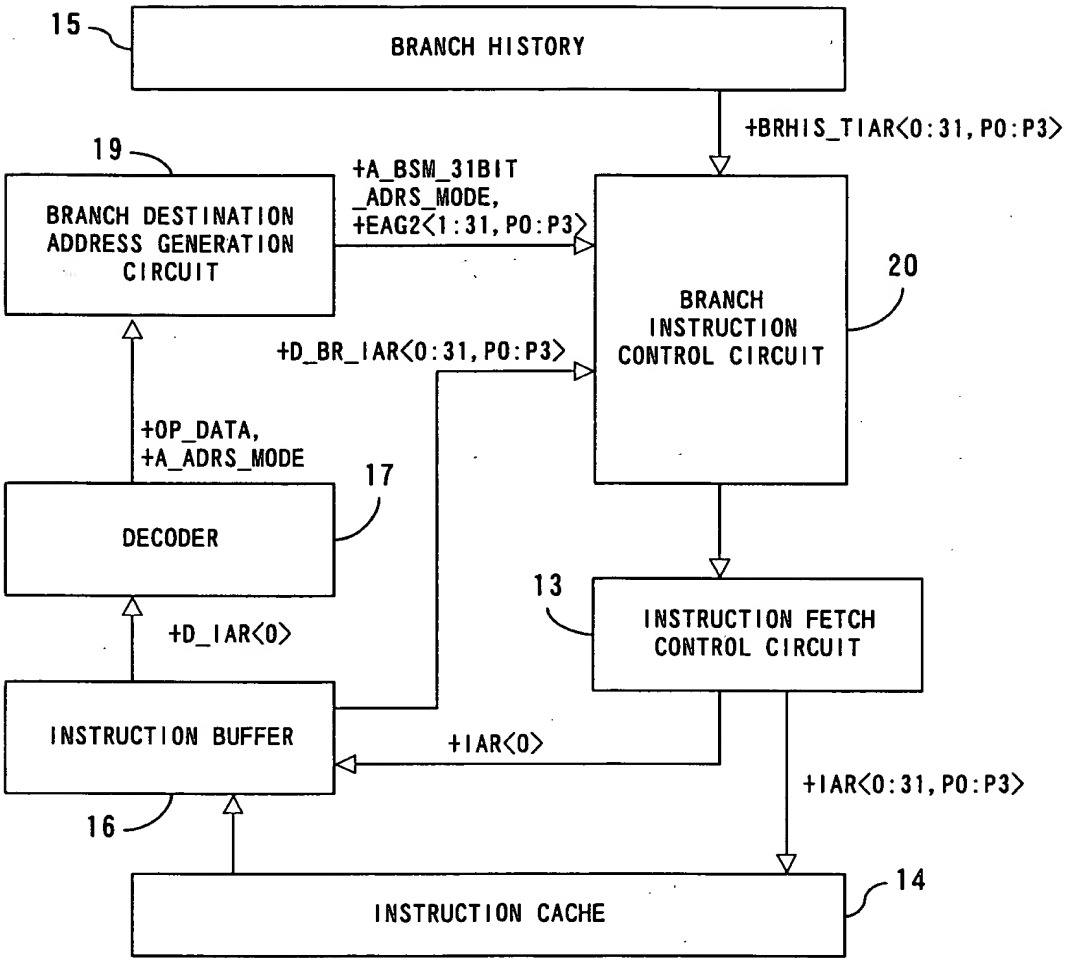

15
BRANCH HISTORY
+BRHIS_TIAR<0:31, P0:P3>
19
BRANCH DESTINATION ADDRESS GENERATION CIRCUIT
+A_BSM_31BIT _ADRS_MODE, +EAG2<1:31, P0:P3>
20
BRANCH INSTRUCTION CONTROL CIRCUIT
+D_BR_IAR<0:31, P0:P3>
+OP_DATA, +A_ADRS_MODE
17
DECODER
13
INSTRUCTION FETCH CONTROL CIRCUIT
+D_IAR<0>
INSTRUCTION BUFFER
+IAR<0>
+IAR<0:31, P0:P3>
16
14
INSTRUCTION CACHE

FIG. 6

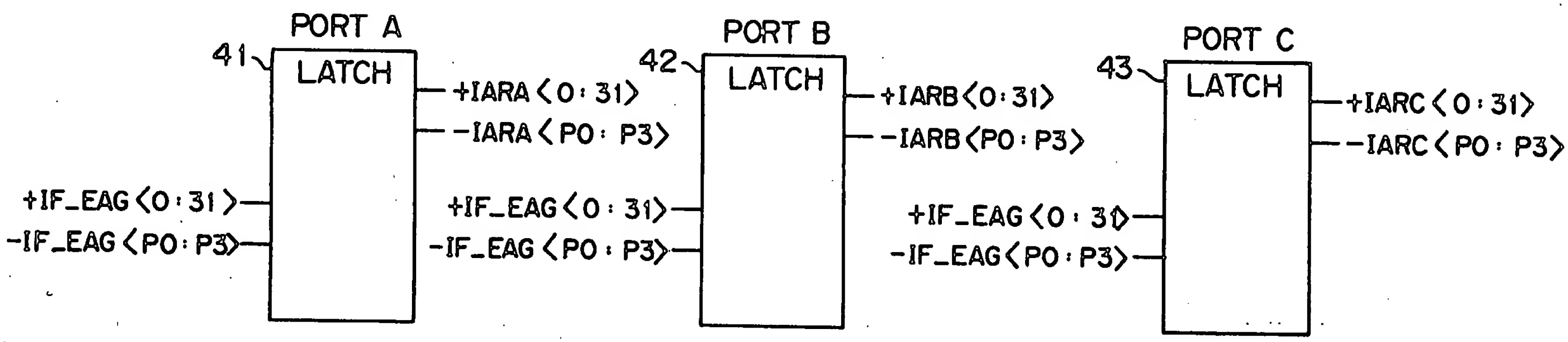
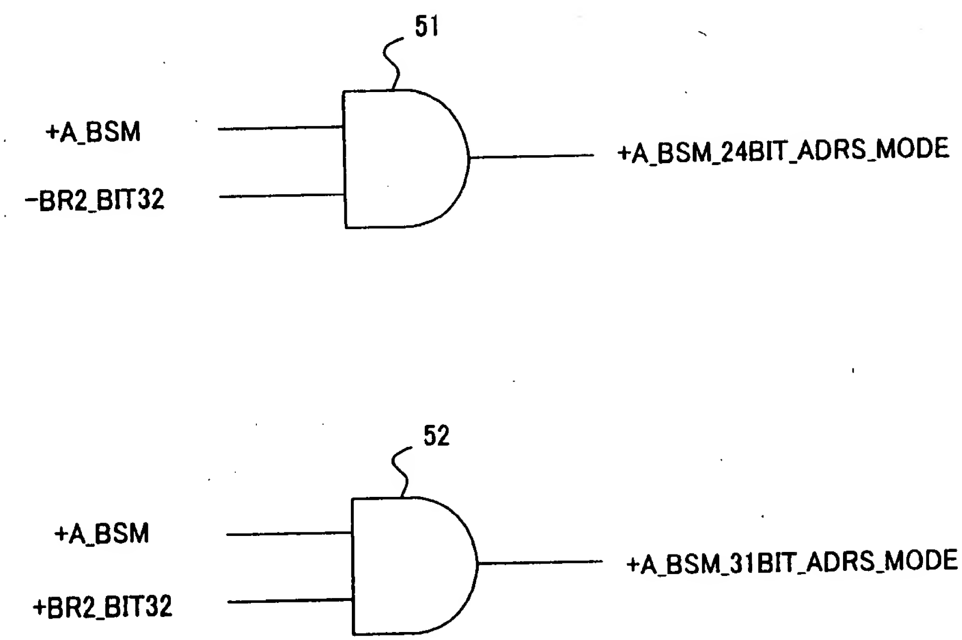

PORT A
41
LATCH
+IF_EAG<0:31>
-IF_EAG<P0:P3>
+IARA<0:31>
-IARA<P0:P3>
PORT B
42
LATCH
+IF_EAG<0:31>
-IF_EAG<P0:P3>
+IARB<0:31>
-IARB<P0:P3>
PORT C
43
LATCH
+IF_EAG<0:31>
-IF_EAG<P0:P3>
+IARC<0:31>
-IARC<P0:P3>

FIG. 7


51
+A_BSM
-BR2_BIT32
+A_BSM_24BIT_ADRS_MODE
52
+A_BSM
+BR2_BIT32
+A_BSM_31BIT_ADRS_MODE

F I G. 8

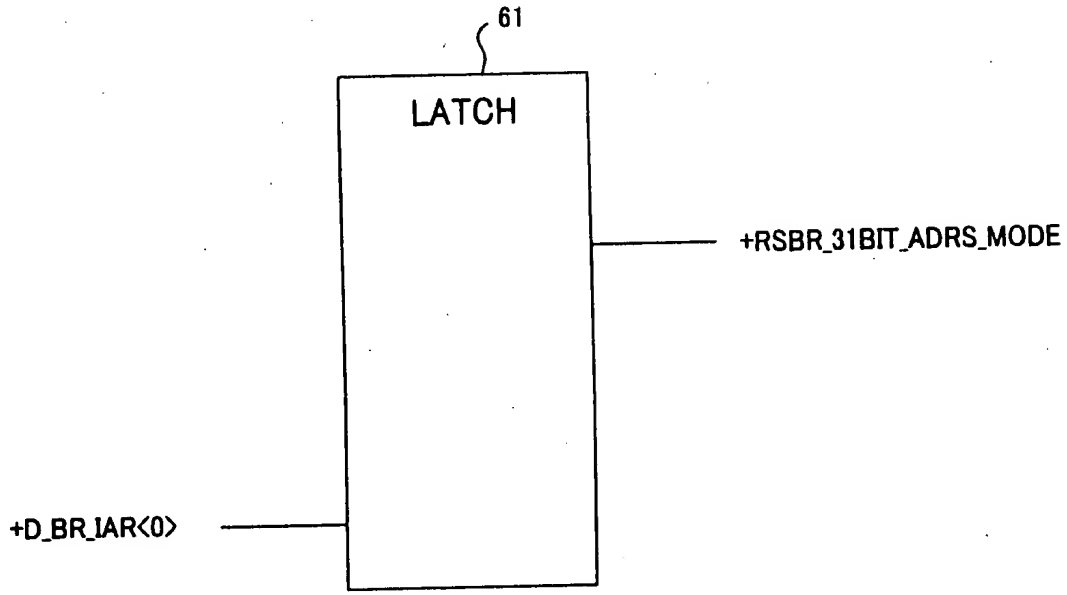


FIG. 9

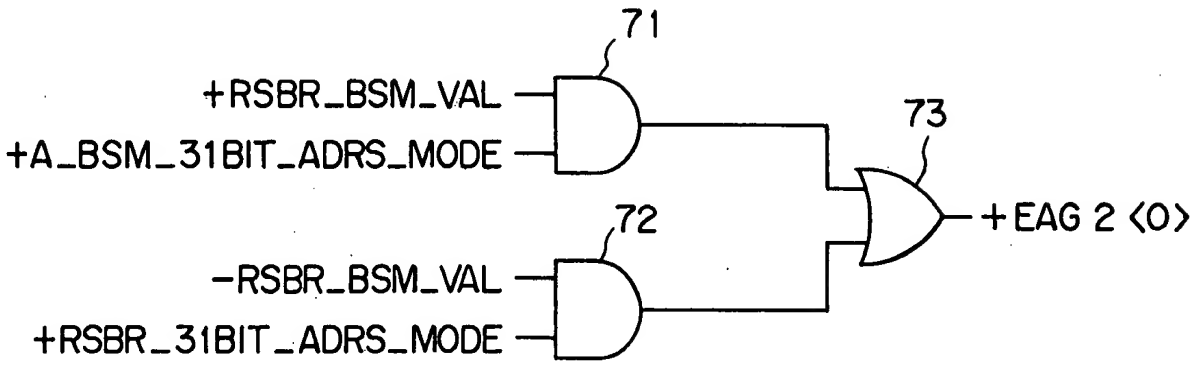


FIG. 10

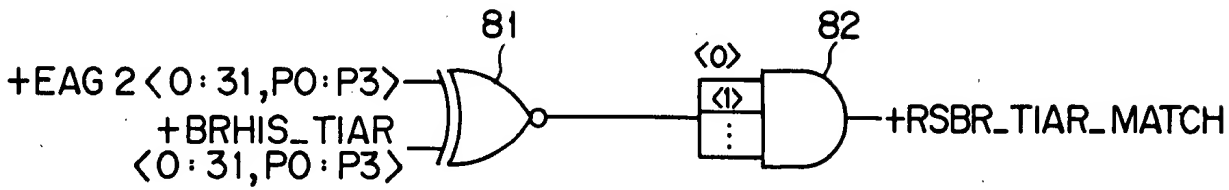


FIG. 11

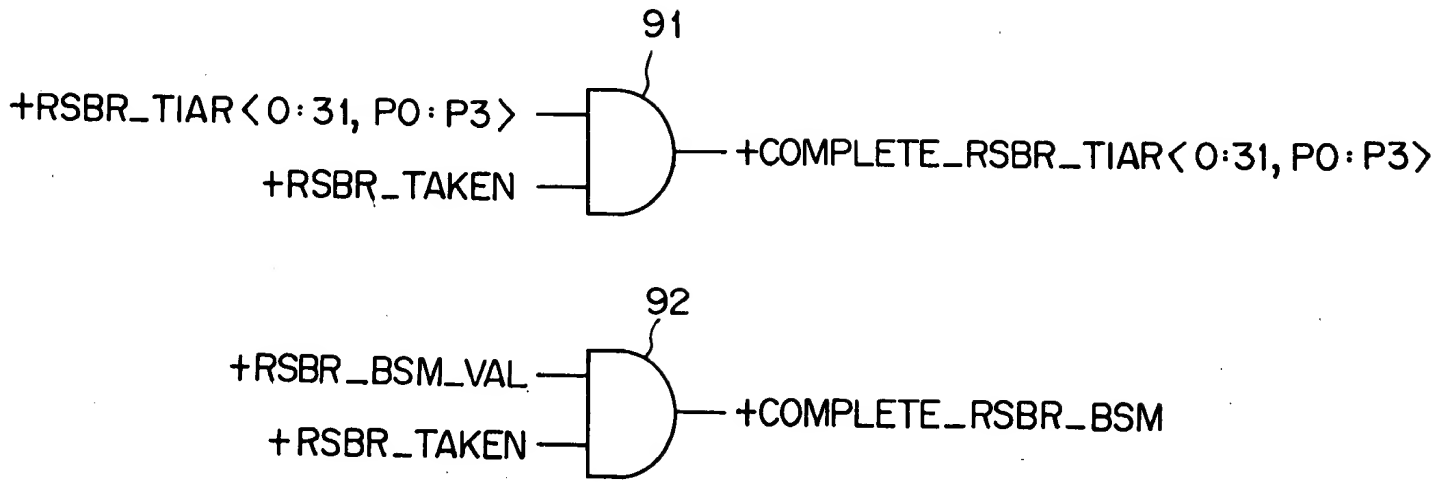

91
+RSBR_TIAR<0:31, P0:P3>
+RSBR_TAKEN
+COMPLETE_RSBR_TIAR<0:31, P0:P3>
92
+RSBR_BSM_VAL
+RSBR_TAKEN
+COMPLETE_RSBR_BSM

FIG. 12